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Cite as: J. Vac. Sci. Technol. B **38**, 033202 (2020); https://doi.org/10.1116/1.5135590
Submitted: 07 November 2019 . Accepted: 18 March 2020 . Published Online: 09 April 2020

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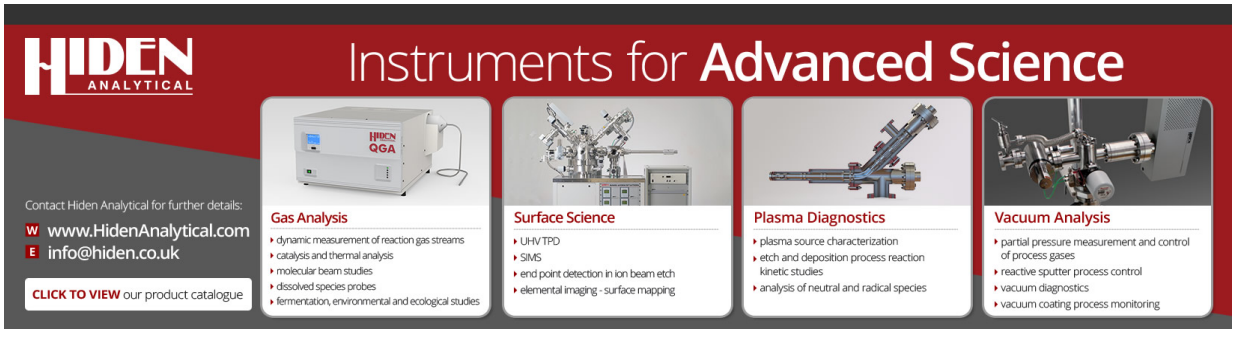

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ABSTRACT

AlGaN polarization-doped field-effect transistors were characterized by DC and pulsed measurements from room temperature to 500 °C in ambient. DC current-voltage characteristics demonstrated only a 70% reduction in on-state current from 25 to 500 °C and full gate modulation, regardless of the operating temperature. Near ideal gate lag measurement was realized across the temperature range that is indicative of a high-quality substrate and sufficient surface passivation. The ability for operation at high temperature is enabled by the high Schottky barrier height from the Ni/Au gate contact, with values of 2.05 and 2.76 eV at 25 and 500 °C, respectively. The high barrier height due to the insulatorlike aluminum nitride layer leads to an I_{ON}/I_{OFF} ratio of 1.5×10^9 and 6×10^3 at room temperature and 500 °C, respectively. Transmission electron microscopy was used to confirm the stability of the heterostructure even after an extended high-temperature operation with only minor interdiffusion of the Ni/Au Schottky contact. The use of refractory metals in all contacts will be key to ensure a stable extended high-temperature operation.

I. INTRODUCTION

One limitation with the current wide bandgap semiconductor GaN and SiC technology is the materials' critical breakdown electric field of 3.9 and 2.5 MV/cm, respectively. A potential advance is the evolution to ultrawide bandgap (UWBG) semiconductors such as Ga_2O_3 or high aluminum content AlGaN. $Al_{0.7}Ga_{0.3}N$ exhibits a critical electric field of 12 MV/cm[1] with a bandgap of 5.4 eV and 4× and 20× greater Johnson Figure of Merit (FOM) ($E_c^2 \cdot V_s^2/4\pi^2$) than GaN and SiC, respectively. Experimentally, $Al_{0.7}Ga_{0.3}N$ transistors have been demonstrated to withstand 3.6 MV/cm, which already exceeds the limits of SiC and nearly matches the theoretical limit of GaN.[2] This result has come early in the developmental stage of AlGaN transistors and shows the high-power potential for AlGaN channel devices; however, this result was limited by a relatively low mobility (90 $cm^2/V\,s$). The performance of AlGaN channel high electron mobility transistors (HEMTs) has demonstrated excellent high-temperature operation and rf performance,[3–7] including operation of $Al_{0.85}Ga_{0.7}N/Al_{0.7}Ga_{0.3}N$ HEMTs to 500 °C with nearly ideal 100 kHz gate lag performance,[3] and f_t and f_{max} of 28.4 and 18.5 GHz, respectively, with the same heterostructure using an 80 nm gate length.[7]

The trade-off with UWBG materials comes with difficulty in attaining low Ohmic contact resistance, high mobility, and high sheet density simultaneously. The route to attain low Ohmic contact resistance has been through unique metallization and regrowth methods.[8,9] To achieve simultaneous high mobility and high sheet density, polarization-doped field-effect transistors (POLFET) have been demonstrated.[10–16] In a traditional GaN HEMT structure, the mobility is limited by the interface of the channel to barrier layer. With a POLFET, there is continuous compositional grading and not an abrupt heterojunction that avoids the issues of interfacial surface roughness.[17] In addition, as the electron flow is primarily in the high aluminum region near the surface, the formation of planar Ohmic contacts is easier than to the barrier layer of high aluminum content AlGaN channel HEMTs.[9] The POLFET is more similar to a traditional field-effect transistor than an HEMT. Armstrong *et al.*[10,11] have reported the room temperature DC performance of $Al_xGa_{1-x}N$

POLFETs with gradings from x = 0.7 to 0.85 and from x = 0.6 to 1. This work showed an improvement in the electron mobility from 210 to 320 $cm^2/V\,s$ in the higher graded sample. Additionally, the polarization-induced doping profile increased from 7×10^{17} to $2.7 \times 10^{18}\ cm^{-3}$.

There are drawbacks for these Al-rich AlGaN heterostructures, including the low thermal conductivity of the ternary alloy that leads to device self-heating.[18] Despite the low thermal conductivity, the on-resistance and maximum drain current of Al-rich AlGaN transistors have been shown to be much less sensitive to high temperatures when compared to GaN high electron mobility transistors.[6] In this work, $Al_xGa_{1-x}N$ POLFETs graded from x = 0.7 to 0.85 on sapphire substrates were operated from 25 to 500 °C in an ambient atmosphere. The devices were characterized by analyzing their DC *I–V* characteristics, gate lag, subthreshold slope, Schottky barrier height (SBH), and other relevant device parameters. Understanding the temperature dependence of these device parameters is the first step to project AlGaN POLFETs' potential for high-temperature performance and to understand whether they will have the potential to supplant HEMT technologies.

II. FABRICATION AND CHARACTERIZATION

POLFET structures were grown at low pressure (75 Torr) by metalorganic vapor phase epitaxy on sapphire substrates in a Veeco D-125 system using trimethylgallium, trimethylammonia, and ammonia as precursors. First, 2.3 μm thick AlN nucleation and buffer layers were grown on the (0001) *c*-plane sapphire misoriented by 0.2° toward the *m*-plane. Then, a 0.25 μm unintentionally doped $Al_{0.7}Ga_{0.3}N$ was grown, followed by the linearly graded 110 nm $Al_xGa_{1-x}N$ from x = 0.7 to 0.85 (Fig. 1). The molar flux of the group III precursors was maintained at a constant value as the compositions were varied. Contactless measurement of the sheet resistance yielded 5500 Ω/□, which combined with Capacitance-Voltage (CV) measurement, gives a carrier density, n_s, of $5.4 \times 10^{12}\ cm^{-2}$. Circular POLFETs were fabricated with a gate length of 2 μm and a symmetric source/drain to gate spacing of 3 μm. The gate circumference was 660 μm. Planar Zr/Al/Mo/Au Ohmic contacts were deposited and subsequently annealed ($\rho_c = 1.1 \times 10^{-3}\ \Omega\,cm^2$). The gate was formed by the deposition of Ni/Au into an opening on the 100 nm thick SiN dielectric to allow for edge termination.

DC characterization was carried out using an Agilent 4156C parameter analyzer using Be/Cu probe tips. An Agilent B114A pulse generator and an Agilent DSO7054B oscilloscope were used to collect pulsed data. A Wentworth automated temperature control chuck was used to vary the chuck temperature from 25 to 500 °C. The chuck provides backside heating, and there is heat loss due to convection, radiation, and imperfect contact of the wafer to the chuck—the deviations between the chuck and device temperature were 0, 2, and 5 °C at the chuck temperatures of 200, 400, and 500 °C, respectively, as confirmed by a contactless IR temperature probe on the surface of the wafer. The device temperatures were adjusted to the set temperatures.

Transmission electron microscopy (TEM) was prepared using the focused ion beam (FIB) lift out technique on an FEI Strata 400 Dual Beam FIB/SEM. Samples were imaged with an FEI Tecnai Talos FEG/TEM operated at 200 kV in the bright-field and high-angle annular dark-field (HAADF) mode. Electron dispersive spectroscopy spectra were acquired in the STEM mode using the FEI Talos 4SCDD system.

III. ELECTRICAL CHARACTERIZATION

In Fig. 2, typical three-terminal current-voltage characteristics are shown at 25, 250, and 500 °C. The POLFETs exhibited good gate control for gate-to-source biases of up to +4 V, with modulation still occurring above this, but with gate leakage becoming a limiting factor. The drain current density reached peak values of 24, 19, and 7 mA/mm at 25, 250, and 500 °C, respectively. The linear current response at low drain bias gave a specific on-resistance of 203 Ω mm at room temperature, indicating good Ohmic behavior of the planar contacts relative for such a high surface Al composition.

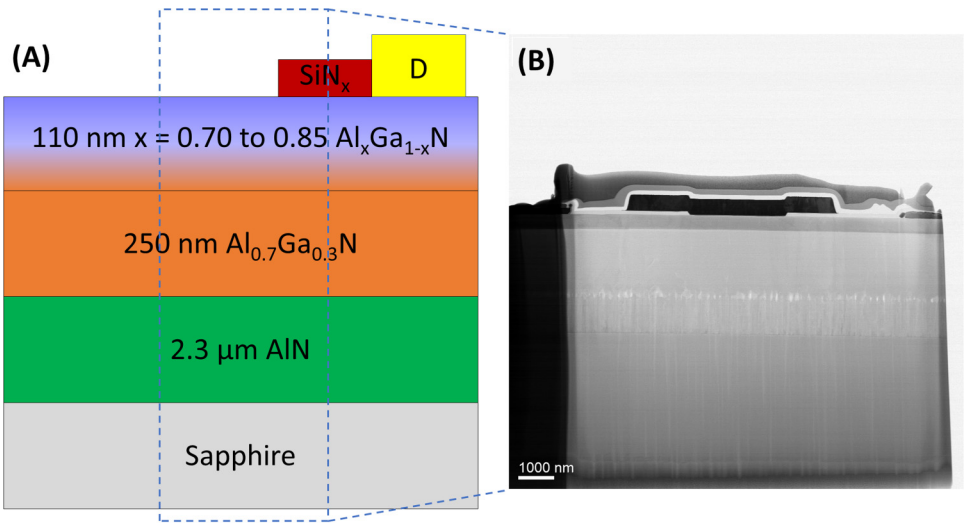

FIG. 1. (a) Device schematic and epitaxial structure of the POLFET and (b) bright-field-TEM image of epitaxial structure with gate contact.

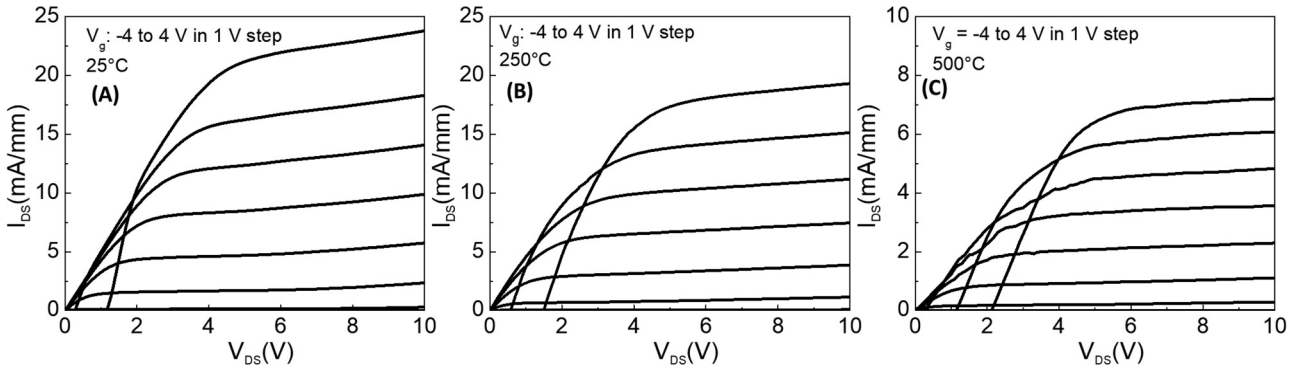

FIG. 2. DC *I–V* characteristics at (a) 25, (b) 250, and (c) 500 °C demonstrate gate modulation and full pinchoff across the entire temperature range.

Using circular Transmission Line Method (TLM) structures, a specific contact resistance of $1.2 \times 10^{-3}\,\Omega\,\mathrm{cm}^2$ was obtained. This planar metallization was previously used for the high Al-content 85/70 HEMT structure, where it was not truly Ohmic.[10] However, in the graded composition from 70% to 85% aluminum, we formed Ohmic contacts without requiring regrowth techniques.[9] This result makes sense as in the HEMT structure the barrier layer is insulator-like and heavily depleted with the electron channel residing usually >20 nm beneath the surface, which gives the need for a regrown contact scheme. While in the case of the POLFET, the polarization provides free carriers at the metal-semiconductor interface. In future works, a regrown contact may assist with achieving contact resistances similar to that of GaN HEMTs on the order of 10^{-6} and $10^{-7}\,\Omega\,\mathrm{cm}^{-2}$, but this is an active area of current study.

Transfer characteristics at 25 and 500 °C are shown in Fig. 3(a) and I_{On}/I_{OFF} as a function of temperature in Fig. 3(b). A nominal change was observed in the deep subthreshold voltage. The drain leakage current of 10 pA/mm was exceptionally low at 25 °C but increased to 20 μA/mm at 500 °C. With heating, electrons gain sufficient energy to surmount the Schottky barrier of the gate, leading to an increase in drain leakage current along with contributions from the bulk. To further investigate the reason for the change in the drain leakage current requires an understanding of the gate characteristics. To analyze the gate characteristics, the thermionic emission model was employed to extract the SBH and the ideality factor,

$$I = I_0 \exp\left(\frac{qV}{nkT}\right)\left[1 - \exp\left(-\frac{qV}{kt}\right)\right], \tag{1}$$

$$I_0 = AA^{**}T^2 \exp\left(-\frac{q\phi_b}{kT}\right), \tag{2}$$

where I_0 is the reverse saturation current, V is the applied voltage, n is the ideality factor, A is the effective diode area, A^{**} is the Richardson constant, and ϕ_b is the SBH.

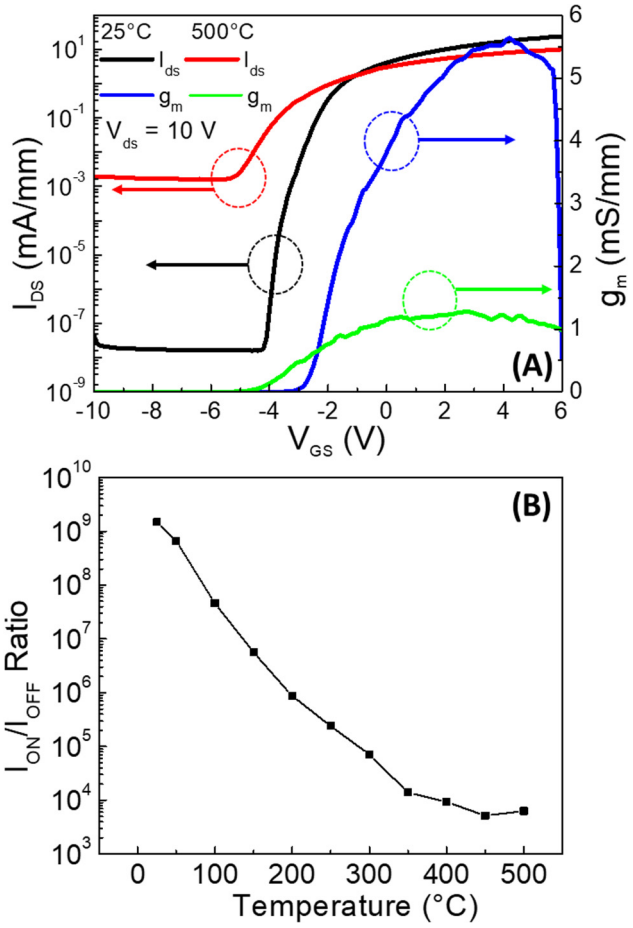

FIG. 3. (a) Transfer characteristics at 25 and 500 °C and (b) I_{ON}/I_{OFF} ratio as a function of temperature.

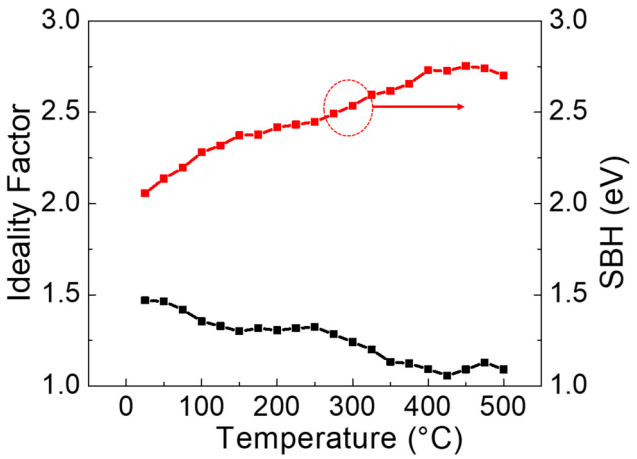

FIG. 4. Schottky barrier height and ideality factor as a function of temperature.

In Fig. 4, at room temperature, we find an SBH of 2.05 eV, which is sufficient to reduce the drain leakage current to $\sim 10^{-11}$ A/mm. The barrier height increase and ideality factor decrease are due to the thermally enhanced ionization of the donor atoms and subsequent drift of electrons to the 3D electron sheet. This drift leads to a widening of the metal-semiconductor depletion region, which directly increases the metal-semiconductor barrier height. However, this trend does not align as well with the observed drain leakage current in Fig. 3 due to the leakage current being dominated by the source leakage current. Finally, the gate stack of Ni/Au does undergo metal reordering after operation at 350 °C and beyond as confirmed by TEM.[3] The initial device performance cannot be recovered if the device has been heated to ≥350 °C.

From the I_d-V_g curves in Fig. 3(a), the subthreshold swing was extracted to evaluate the ideality of the devices, as shown in Fig. 5. A subthreshold swing of 110 and 666 mV/dec. were obtained at 25 and 500 °C, respectively. An approximation of the interfacial trap density was extracted using the following differentiated relation:[19]

$$\frac{dS}{dT} = \frac{k}{q}\ln(10)\left(1 + \frac{D_{it}q}{C_{int}}\right), \tag{3}$$

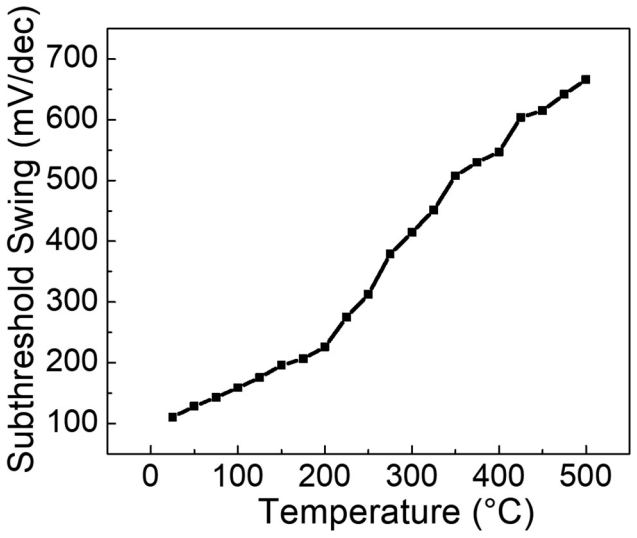

FIG. 5. Subthreshold swing as a function of temperature has two distinct linear regimes.

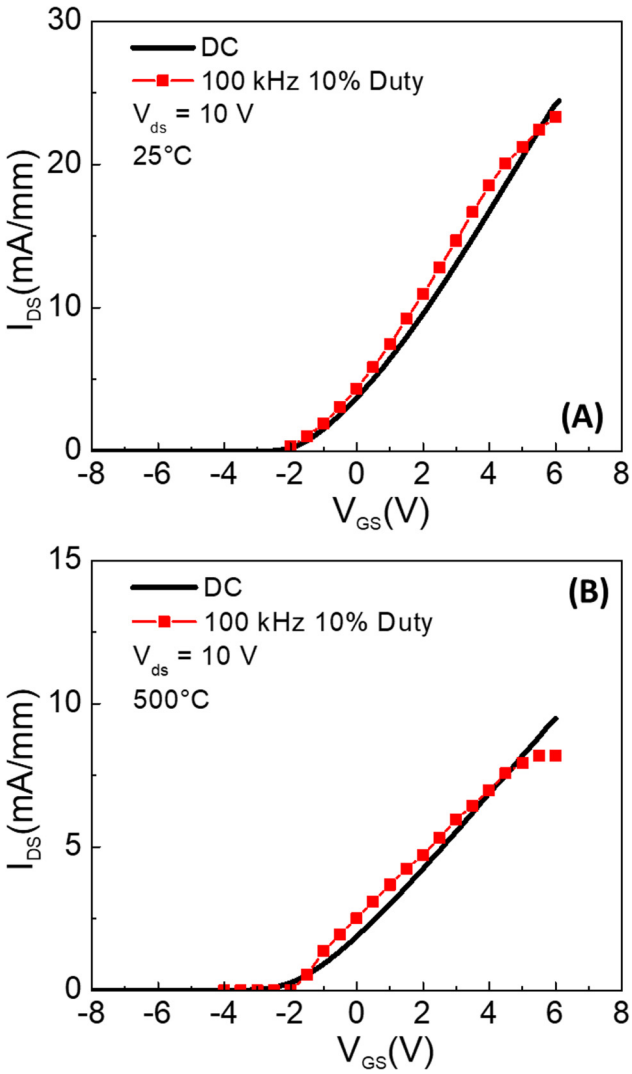

FIG. 6. DC and gate lag performance at (a) 25 and (b) 500 °C at 100 kHz and 10% duty under V_{ds} = +10 V with the gate switching from V_{gs} = −6 V to the data point.

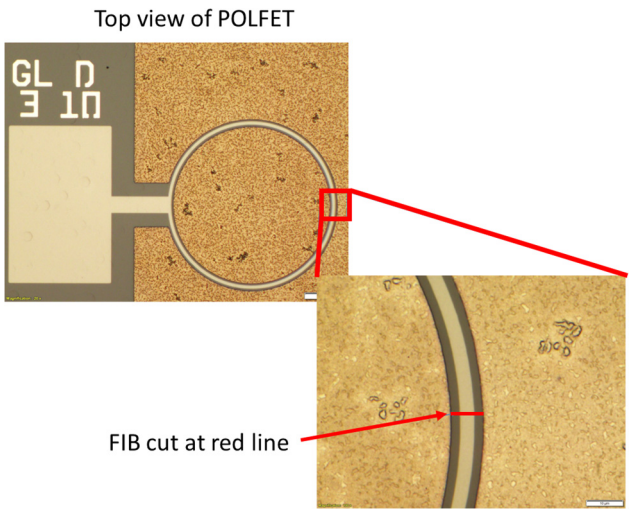

FIG. 7. Top view of POLFET and FIB cut location.

where S is the subthreshold wing, T is the temperature, k is the Boltzmann constant, q is the elementary charge of an electron, D_{it} is the interfacial trap density, and C_{int} is the surface depletion capacitance. From Fig. 5, two linear regimes are visible: 25–200 °C and 200–500 °C with trap densities of 1.85×10^{11} and 1.91×10^{12} $cm^{-2}\,V^{-1}$, respectively. Thermal excitation of trap states is expected and will be partially responsible for worsening of leakage currents at elevated temperature with trap assisted tunneling.

Since high-power switching is a potential application, the POLFETs were evaluated under a gate switching operation of 100 kHz at 10% duty. The gate lag measurement was carried out under drain bias of +10 V and switching the gate voltage from −6 to the data point (Fig. 6). At 25 °C, the pulsed performance exceeds that of DC due to reduced channel heating under switched operation. Once the device is heated to 200 °C, the pulsed performance matched DC. At 500 °C, only very slight reduction in pulsed drain current is noted under high gate voltage. These results are promising for low frequency power switching and indicate that few trap states form a virtual gate. The gate lag and subthreshold swing extraction of interfacial trap density indicate high-quality epitaxial

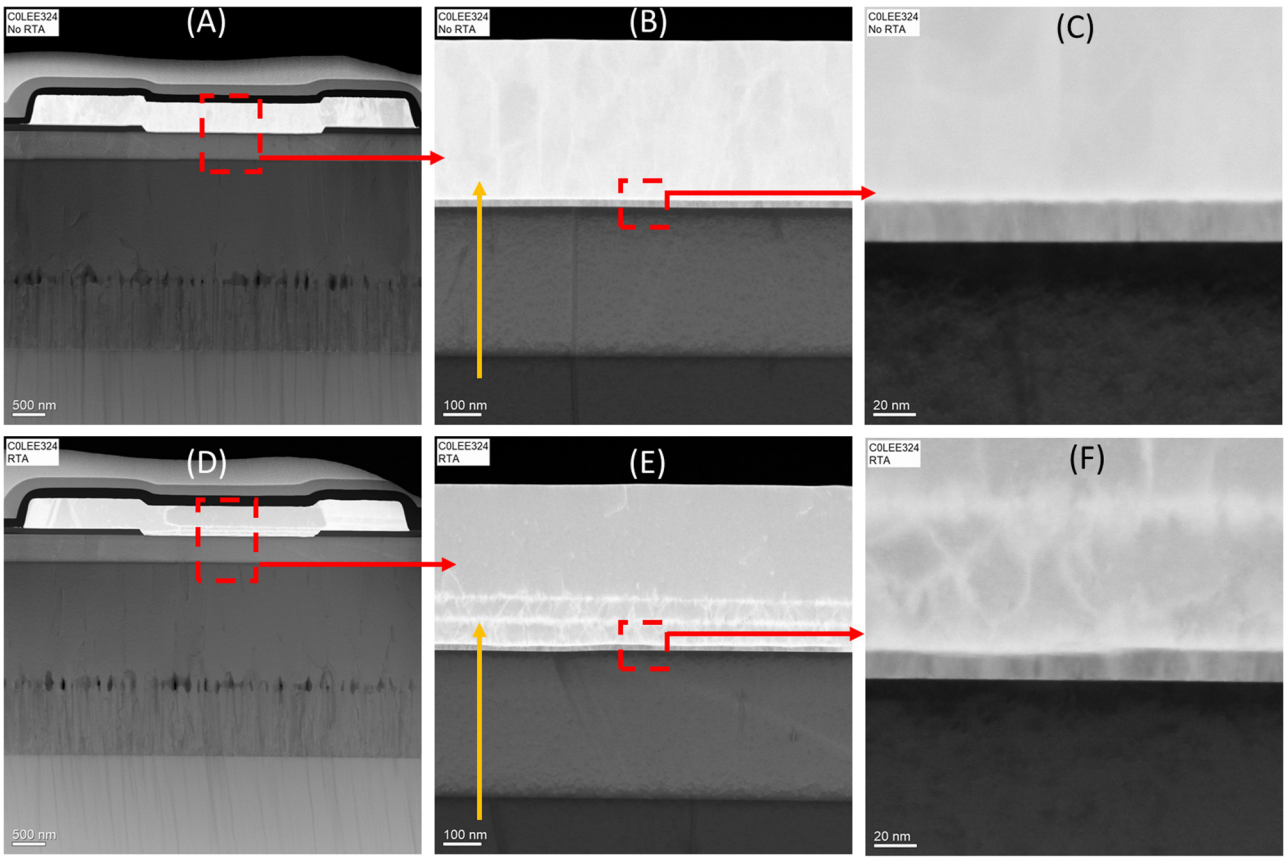

FIG. 8. HAADF TEM image of (a) fresh device and (d) 500 °C treated device, with a further magnification of the Schottky metal/AlGaN interface of the fresh device [(b) and (c)] and 500 °C operated device[(e) and (f)]. The yellow arrow indicates the location and direction of EDS scans.

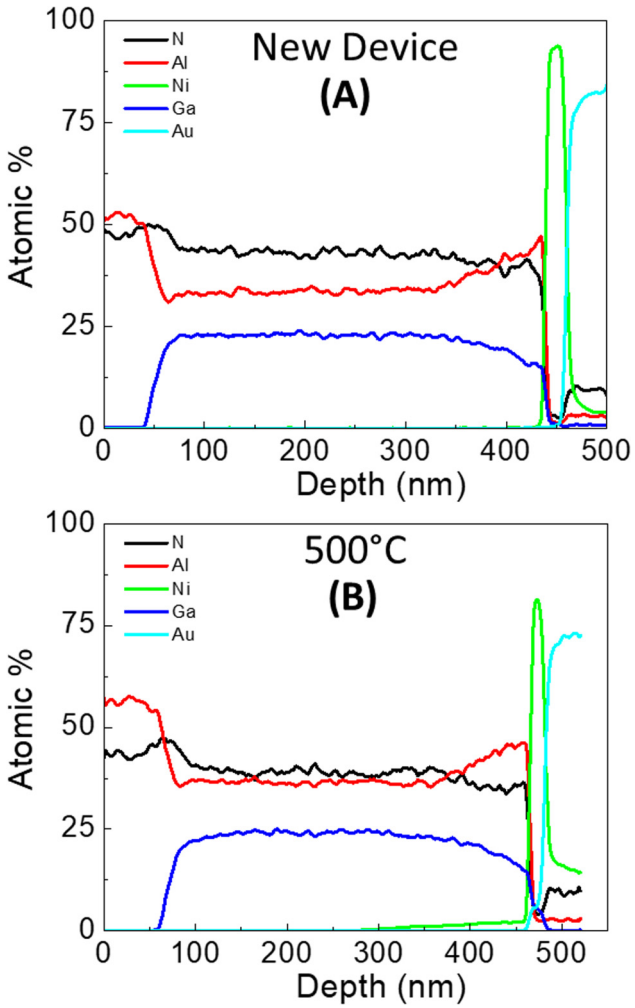

FIG. 9. EDS spectra of a (a) new device and a (b) 500 °C operated device.

growth, low-defect gate metal to semiconductor interface, and effective surface passivation. The latter is a concern with the POLFET electron channel being near the surface and being more susceptible to surface states than traditional HEMTs.

For high frequency switching, maintaining high mobility is important to ensure that saturation velocity can be reached. The benefit of a POLFET structure is the removal of ionized impurity scattering as no dopant such as Si is added. However, as the flow is within a 3D electron slab of a ternary alloy the effects of alloy scattering are significant.

IV. STRUCTURAL CHARACTERIZATION

TEM and Electron Dispersive Spectroscopy (EDS) characterization were performed to gain a better understanding and confirm the structural integrity of the POLFET throughout the high-temperature testing. Figure 7 shows the FIB cut location for the subsequent images and analysis.

A primary danger of prolonged high-temperature operation is instability at heterointerfaces. The two primary locations of concern are the graded active channel from $Al_{0.7}Ga_{0.3}N$ to $Al_{0.85}Ga_{0.15}N$ and the gate metal contact to the top of the active channel. Figure 8 presents an HAADF TEM image of a fresh device [(a)–(c)] and a device that had been subject to 500 °C testing [(d)–(f)] in the gate area. The only distinct change is in that of the gate metal [Figs. 8(c) and 8(d)], where grains within the Au top layer of the Schottky metal are apparent. These grains are likely the intermixing of the Ni/Au Schottky metal, as they are primarily present near the interface and do not initially appear to extend to the surface of the Au metal. Slight changes in the thin Ni layer uniformity are noted in the further magnified images [Figs. 8(e) and 8(f)] as compared to the fresh device [Figs. 8(b) and 8(c)], with an approximate thinning of the Ni layer at the interface by 35%. Diffusion traces of the Ni intermixing with the Au become apparent in Fig. 8(f).

While visually it is simple to observe changes in the metallization, visual inspection of the graded layer is more challenging. To identify if changes in the active layer were present, EDS was employed; the vertical arrows on Figs. 8(b) and 8(e) show the scan direction on each sample. Figure 9 presents the EDS spectra comparing the Al, Ga, N, Ni, and Au atomic percentages as a function of depth for both a fresh device and 500 °C operated device. No change is noted in the aluminum, gallium, or nitrogen depth profile after a high-temperature operation. The only shift is within the Schottky contact, namely nickel, which drops in peak atomic % and is found to have diffused into the Au above, confirming our previous conclusions from the TEM images.

V. CONCLUSIONS

In summary, DC and pulsed characterization from 25 to 500 °C of $Al_xGa_{1-x}N$ POLFETs with grading from $x = 0.7$ to 0.85 showed full gate modulation and pinchoff regardless of the operating temperature. The I_{ON}/I_{OFF} ratios of $\sim 10^9$ and $\sim 10^4$ were achieved at 25 and 500 °C, respectively. The 100 kHz switching operation across the entire temperature range showed a near ideal operation with only the slight formation of a virtual gate at high gate voltages and high temperature. Even without optimization of passivation, the influence of surface states was low. The primary limiting factor for this structure is electron mobility, which can be improved with grading to entirely AlN at the surface. In its current state, this technology is very promising for medium frequency high-power applications as it presents itself with very little difference in terms of processing techniques from that of current GaN technologies. However, reduction of leakage current at high temperatures will be a subject of further inquiry as the technology in this state is equal to GaN.

ACKNOWLEDGMENTS

This work was supported by the Laboratory Directed Research and Development Program at Sandia National Laboratories. Sandia National Laboratories is a multimission laboratory managed and operated by National Technology and Engineering Solutions of Sandia, LLC, a wholly owned subsidiary of Honeywell International, Inc., for the U.S. Department of Energy's National Nuclear Security

Administration under Contract No. DE-NA-0003525. The views expressed in the presentation do not necessarily represent the views of the U.S. Department of Energy or the United States Government. The work at the University of Florida was partially sponsored by the Department of the Defense, Defense Threat Reduction Agency (No. HDTRA1-17-1-011), monitored by Jacob Calkins.

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